2T1R REGULATED MEMRISTOR CONDUCTANCE CONTROL ARRAY ARCHITECTURE FOR NEUROMORPHIC COMPUTING USING 28 NM CMOS TECHNOLOGY

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1. MOTIVATION

- Computing in memory (CIM) is an innovative computing paradigm, where the computation and storage occur in situ
- Memristors arranged in a crossbar array pattern emulate vector matrix multiplication operations and exhibit high parallelism [1]

The motivation of this work is to implement a conductance control array with regulated sources having the following advantages:

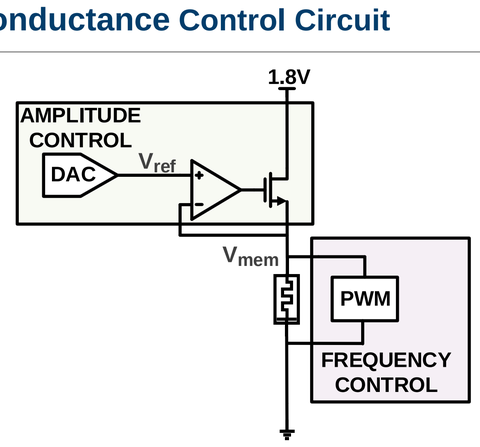
- Reduce the noise effects by rectification of line resistances and potential divider effects in a regular crossbar scheme [2] and restriction of sneak path current [3]
- Application of a differential voltage across memristors and thus removing virtual ground scenario [4]

2. APPROACH

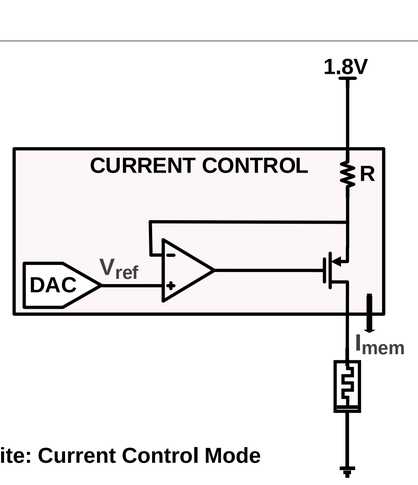
The objective includes:

- A comparative study of the voltage mode and current mode conductance control techniques
- Development of a computing architecture in 28nm CMOS technology

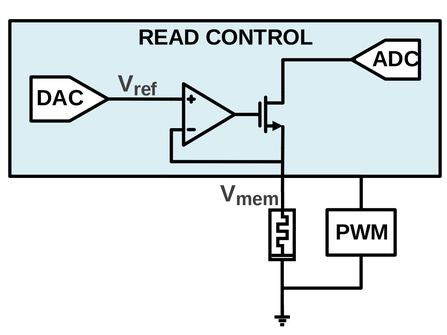
Conductance Control Circuit



Write: Voltage Control Mode



Write: Current Control Mode

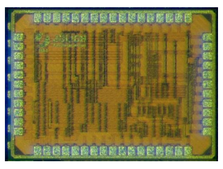


Read Mode

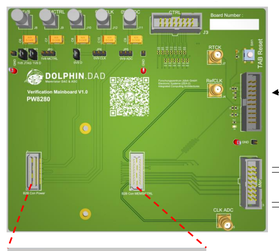
- Microarchitecture in this work includes two control modes of operation:
  - i. Voltage Control Mode
  - ii. Current Control Mode
- The regulated voltage/current source signal is applied across/through the memristor, via voltage/current regulator in voltage/current control mode.

3. TAPED OUT CHIP AND PROPOSED MEASUREMENT SETUP

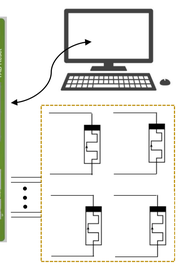
Taped Out Chip



Verification Boards with MCTRL Chip

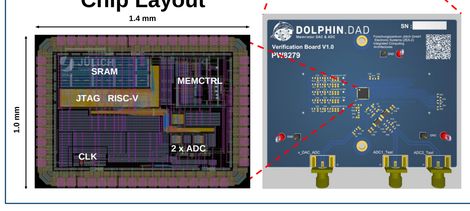


JTAG Interface



Memristor Array

Chip Layout



- Read write verify algorithm is proposed to be implemented using integrated RISC-V architecture.
- A JTAG interface provides digital configurations and pulse width generator set bits for conductance control architecture.

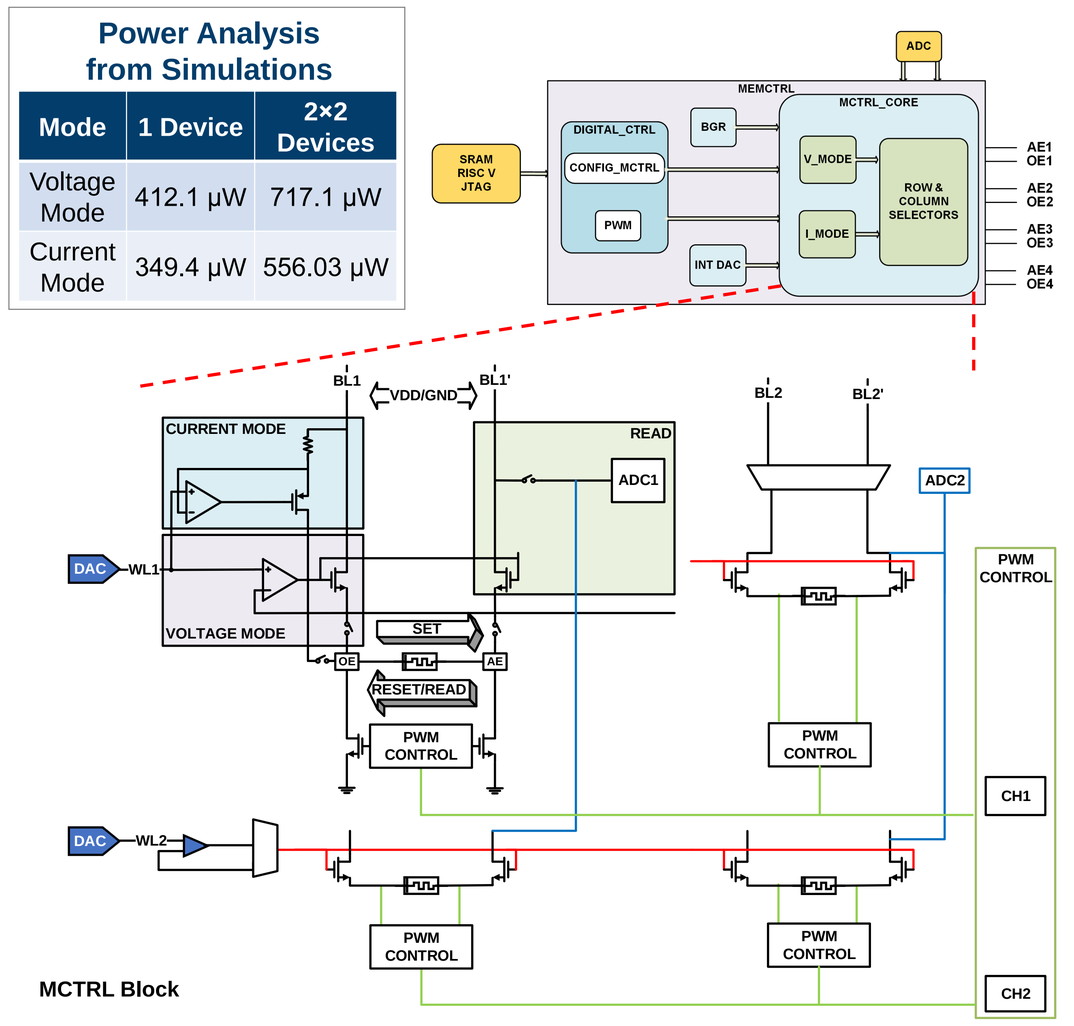
4. DESIGN IMPLEMENTATION AND SIMULATION RESULTS

MCTRL Block

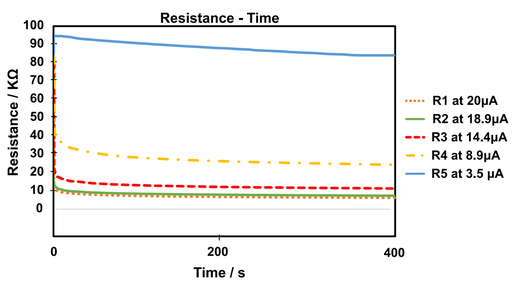
- 2T1R Architecture for memristor array is introduced, where analog conductance state could be obtained by adjusting pulse width and pulse amplitudes or controlling the current through the memristor.
- The memristors are not co-integrated in this architecture, however, pins are provided for accessing external memristors.

Power Analysis from Simulations

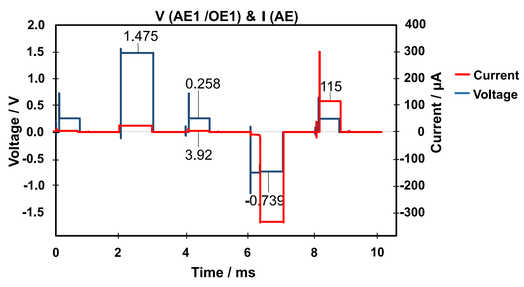
Mode	1 Device	2×2 Devices
Voltage Mode	412.1 µW	717.1 µW
Current Mode	349.4 µW	556.03 µW



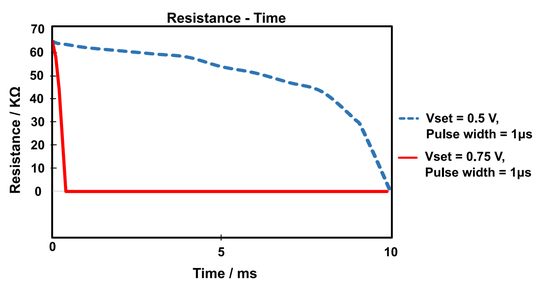
MCTRL Block



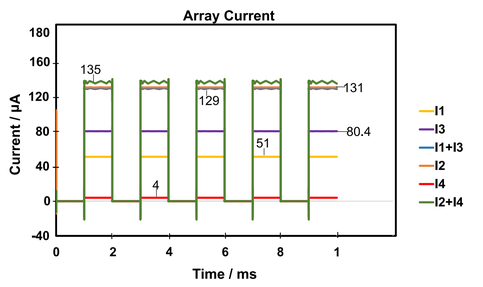
Resistance Variation in Current Mode



Read Verify Algorithm With Layout Parasitics



Resistance Variation in Voltage Mode



2 x 2 Array Current with Layout Parasitics

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[1] H. Bao et al., “Toward memristive in-memory computing: principles and applications”, Frontiers of Optoelectronics, vol. 15(1), 23, 2022
[2] W. L. Ahmad et al., “Analysis of VMM Operations on 1S1R Crossbar Arrays and the Influence of Wire Resistances”, IEEE ISCAS, 91-95, 2022
[3] L. Shi et al., “Research progress on solutions to the sneak path issue in memristor crossbar arrays”, Nanoscale Adv., vol. 2(5), 1811–1827, 2020
[4] J. Chen et al., “Multiply accumulate operations in memristor crossbar arrays for analog computing”, J. Semicond., vol. 42(1), 013104, 2021